AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) An apparatus comprising:

a branch indication memory having a plurality of memory locations to store branch indication information for each of a plurality of states at each of a plurality of sections, the branch indication information indicating a branch that is most likely to lead to a state;

a memory address logic in communication with the branch indication memory, the memory address logic to indicate a subset of the plurality of memory locations, the subset including memory locations to store branch indication information for each of the plurality of states at an indicated section;

a selector in communication with the branch indication memory, the selector to receive the branch indication information for each of the plurality of states at the indicated section, the selector to select a portion of the received branch indication information based on selection information; and

a shift register in communication with the selector, the shift register including a plurality of register segments to store information, the plurality of register segments including a first segment in communication with the selector to receive and store the selected portion of the branch indication information, the shift register in communication with the selector to provide the information stored in the plurality of register segments to the selector as the selection information.

2. (Original) The apparatus of claim 1, wherein the memory address logic comprises a down counter.

3. (Original) The apparatus of claim 1, wherein the plurality of register segments of the shift register comprise a number of register segments that is based on a number of states of a trellis.

4. (Original) The apparatus of claim 1, wherein the plurality of register segments of the shift register comprise (k-1) segments, where k is the constraint length, and wherein the number of states comprises $2^{(k-1)}$ states.

5. (Original) The apparatus of claim 1, implemented in a portable radio communication device comprising a Flash memory.

6. (Original) The apparatus of claim 1, implemented in a cell phone comprising a GSM transceiver.

7. (Original) The apparatus of claim 1, implemented in a computer system comprising a DRAM memory.

8. (Currently Amended) An apparatus comprising:

a branch indication memory to store branch indication information for a state at a section of a plurality of sections of the branch indication memory, the branch indication information indicating a branch that leads to the state;

a memory address logic comprising a counter in communication with the branch indication memory to indicate the section with a value of the counter, the section including the branch indication information for the state and branch indication information for other states at the indicated section;

a selector in communication with the branch indication memory to receive the branch indication information for the state at the indicated section and the branch indication information for the other states at the indicated section, the selector to select the branch

indication information for the state instead of the branch indication information for the other states at the indicated section based on received selection information;

a shift register in communication with the selector to provide information stored in a plurality of register segments to the selector as the selection information, and to receive and store the selected branch indication information.

9. (Cancelled)

10. (Original) The apparatus of claim 8, wherein the selector comprises a multiplexer.

11. (Original) The apparatus of claim 8, wherein the plurality of register segments of the shift register comprise a number of register segments that is based on a number of states of a trellis.

12. (Original) The apparatus of claim 11, wherein the number of register segments is based on a constraint length.

13. (Original) The apparatus of claim 12, wherein the number of register segments comprises (k-1) segments, where k is the constraint length, and wherein the number of states comprises $2^{(k-1)}$ states.

14. (Currently Amended) The apparatus of claim 8, implemented in a portable radio communication device comprising a Flash memory coupled with the apparatus to store information.

15. (Currently Amended) The apparatus of claim 8, implemented in a cell phone comprising a GSM transceiver coupled with the apparatus to receive data from a communications system and provide the data to the apparatus.

16. (Currently Amended) The apparatus of claim 8, implemented in a computer system comprising a DRAM memory coupled with the apparatus to store information.

17. (Original) An apparatus comprising:

a DRAM memory to store information;

a communication device to receive information from a communication system; and

a decoder to perform error correction on the information received from the communication system, the decoder comprising:

a branch indication memory to store branch indication information for a state at a section, the branch indication information indicating a branch that leads to the state;

a memory address logic in communication with the branch indication memory to indicate the section;

a selector in communication with the branch indication memory to receive the branch indication information for the state at the indicated section, the selector to select the branch indication information based on received selection information; and

a shift register in communication with the selector to provide information stored in a plurality of register segments to the selector as the selection information, and to receive and store the selected branch indication information.

18. (Original) The apparatus of claim 17, wherein the memory address logic comprises a down counter.

19. (Original) The apparatus of claim 17, wherein the plurality of register segments of the shift register comprise a number of register segments that is based on a number of states of a trellis.

20. (Original) The apparatus of claim 19, wherein the number of register segments comprises (k-1) segments, where k is the constraint length, and wherein the number of comprises $2^{(k-1)}$ states.

21. (Currently Amended) A method comprising:

storing branch indication information in a branch indication memory having a plurality of sections;

selecting a section of the branch indication memory with a value of a counter;

outputting from the branch indication memory a plurality of branch indication information each for a different state;

selecting a particular branch indication information of the plurality of branch indication information for a particular state of the plurality of states at the selected section based on information that is stored in a shift register;

storing the selected branch indication information in the shift register; and

shifting the branch indication information out of the shift register in order to recover decoded and error corrected information.

22. (Cancelled)

23. (Original) The method of claim 21, wherein selecting the branch indication information for the state comprises using k-1 bits of information stored in the shift register to uniquely select the branch indication information for the state out of a larger set of branch indication information for $2^{(k-1)}$ unique states.

24. (Currently Amended) The method of claim 21, further comprising providing the decoded information to an apparatus that is selected from the group consisting of a computer system

comprising a DRAM memory coupled with the apparatus to store information, a portable radio communication device comprising a Flash memory coupled with the apparatus to store information, and a cell phone comprising a GSM transceiver coupled with the apparatus to receive data from a communications system and provide the data to the apparatus.

25. (Currently Amended) An article comprising:

a storage medium having stored thereon data representing sequences of instructions that if executed cause a decoder to:

store branch indication information in a branch indication memory having a plurality of sections;

select a section of the branch indication memory based on a value of a counter;

provide from the branch indication memory branch indication information for a plurality of different states;

select branch indication information for a state of the plurality of different states at the selected section based on information that is stored in a shift register;

store the selected branch indication information in the shift register; and

shift the branch information out of the shift register in order to recover decoded and error corrected information.

26. (Cancelled)

27. (Currently Amended) The article of claim 25, wherein the instructions further comprise instructions that if executed cause the decoder to:

provide the decoded information to an apparatus that is selected from the group consisting of a computer system comprising a DRAM memory coupled with the apparatus to store information, a portable radio communication device comprising a Flash memory coupled with the apparatus to store information, and a cell phone comprising a GSM transceiver coupled with the apparatus to receive data from a communications system and provide the data to the apparatus.